

UNIVERSITY OF DETROIT MERCY
EE364 – DIGITAL LOGIC CIRCUITS I (3:3:0)
Term I, 2004-2005

Course Description: (Co-requisite: EE365) Binary numbers and arithmetic. Fundamentals of Boolean algebra. Basic logic circuit concepts. Karnaugh maps. Multiplexers, decoders, PLD. Flip-flops, counters. Design of sequential circuits, computer modeling and simulation of digital systems.

Instructor: Dr. Nizar Al-Holou, Professor, E 331/330, 993-3365, alholoun@udmercy.edu
Office Hours: Monday: 1-5, Tuesday: 11-12, Thursday: 3:30-5:30 PM, and anytime my office door is open; or email/call to schedule an appointment.

Course Web page: <http://knowledge.udmercy.edu/>

Lecture: **TR 2:00-3:15 PM, Room E237.**

Course Objective: The primary objective of this course is to study Boolean algebra and its application which provides the basic mathematician tool needed to analyze and synthesize an important class of switching networks. Starting from problem statement, you will learn to design networks of logic gates which have a specific relationship between input and outputs. Then you will study the logical properties of flip-flops, which serves as memory devices in sequential switching networks. By combining flip-flops with gates, you will learn how to design counters, adders, sequence detectors and similar networks.

Required Text: Fundamentals Of Logic Design, Charles H. Roth, Jr., Thompson, 5th edition, 2004.

Required Materials: Engineers Computation Pad (available in Bookstore)

Prerequisites by Topic: Algebra, non-decimal number systems

Learning outcomes:

Upon the successful completion of this course, you will be able to:

- Perform basic arithmetic functions in the binary number system
- Analyze and design gate-level combinational logic circuits
- Use MSI chips to design and implement combinational logic circuits
- Analyze and design sequential state machines using flip-flops
- Analyze and design sequential circuits using MSI circuits such as counters and registers
- Use PLD's to implement combinational and sequential circuits
- Perform computer simulations of designed circuits using MAX+PLUS II
- Use Boolean Algebra to simplify logic functions
- Use K-maps to simplify logic functions
- Use VHDL to describe simple logic circuits

Highlights of Course:

Web Resources: This course has a web site at:

<http://knowledge.udmercy.edu>

Important announcements and other resources will be available on the web site. It should be consulted

frequently, since updates are made regularly. Note in particular that the site has an electronic discussion feature that allows you to ask and answer questions about the course.

- Computer Aided Logic Design and Simulation: The Altera MAX+PLUS II software as well as LogicAid will be used for the simulation of logic circuits and for programming PLD's. You can get a free student version of this package.

Requirements:

Attendance/Participation: Attendance, while not strictly required, can have an impact on the grade for the course. If a student misses class on a day during which a pop quiz is taken, the student will be given a zero for that assignment. Participation in the web-based discussion for the course is encouraged.

Pre-class reading assignments: Students are expected to read assigned sections in the text **before** the class in which the topic is presented.

Homework: This component includes individual homework as well as group assignments. Use of word processing, spreadsheet and simulation programs may be required for some of the assignments.

Homework problems must be done neatly in pencil and on sheets of paper (front only) from an Engineers Computation Pad. For group assignments, only one copy is to be handed in for grading. For individual work, each student must turn in his/her own original work: academic dishonesty will not be tolerated! Homework is due at the **beginning** of the class on the day on which it is due. No late homework will be accepted. Check the web page frequently to see what homework assignments have been made and when they are due.

- In-class assignments: There may be occasional assignments to be completed in class. Scores from these assignments will be recorded as homework. These in-class assignments cannot be made up.

- Quizzes: A number of brief quizzes will monitor your compliance with reading and homework assignments. These quizzes may be **unannounced**, and may take place at the beginning of the class period, so your on-time attendance is critical. There will be no make-up quizzes given for any reason.

- No late homework or make-up exams exceptions make only under compelling circumstances. Should a legitimate emergency arise, a make-up may be negotiated, provided the student notifies me before (preferable) or no more than 24 hours after the time of the scheduled exam. This notification may take place in person, by phone message, or by e-mail (preferred).

Grade: The final grade will be determined from the following components:

1.	Midterm Exam, 10/21/03	20%
2.	Homework	15%
3.	Quizzes	20%
4.	Final Exam	30%
5.	Project	15%

Grading Scale: A 93-100, A- 89-92, B+ 85-88, B 80-84, B- 75-79, C+ 70-74, C 65-69, C- 60-64, D+ 55-59, D 50-54, F 0-49

Academic Integrity: Students are expected to conform to high standards of honesty and integrity in this course. Please refer to the University Catalog and E&S Student Handbook for further explanation of academic integrity.

Important Dates:

October 1 Last day to drop without a "W"
November 22 Last day to withdraw from class

ACADEMIC INTEGRITY: Everything submitted for grading is expected to be a student's own work. Anything suspected otherwise will be dealt with according to the College policy - see the Engineering Science Student Handbook.

TOPICS:

1. Introduction to number systems and conversion, binary arithmetic and codes. (2 hours)
2. Boolean algebra. (3 hours)
3. Algebraic simplification, minterm-maxterm expansions, truth table, conversion of the description of a problem into an algebraic expression. (3 hours)
4. Karnaugh maps, incompletely specified functions. (3 hours)
5. Multi-level design, multiple-output design. (3 hours)
6. Combinational circuit design, fan-in and fan-out, gate delay, timing diagram, hazard in combinational circuits. (2 hours)
7. MSI and LSI circuits and their applications, multiplexers, decoders, adders, read-only memories, programmable logic devices. (4.5 hours)
8. Introduction to VHDL. (1.5 hour)
9. Sequential machine fundamentals: Basic concepts of sequential circuits, SR, T, JK, D flip-flops. (3.5 hours)
10. Design of Registers and Counters. (1.5 hours)
11. Analysis of sequential machines: Signal tracing, timing charts, state tables and graphs. (3.5 hours)
12. Design of sequential machines: sequence detectors, and more complex design problems, system level design concepts. (4 hours)
13. Sequential design optimization: reduction of state tables, state assignment, incompletely specified state tables. (1.5 hours)
14. Sequential design with MSI circuits, programmable logic devices. (3.5 hours)
15. VHDL for Sequential Circuits. (2.5 hours)